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A Network-on Chip Architecture for Optimization of area and power with Reconfigurable Topology on FPGAs

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ABSTRACT: *This is a Network-on-Chip (NoC) architecture enables the network topology to be reconfigured.This enables a general System-on-Chip (SoC) platform, which is currently running on the chip. The topology is configured using energy- efficient topology switches based on physical circuit-switching The ReNoC architecture design shows a 56% decrease in power consumption compared to a static 2D mesh topology*

KEYWORDS: *SOC, NOC, power efficient, VOPD application*

I. INTRODUCTION

Every new CMOS technology generation enables the design of larger and more complex systems on a single integrated circuit. The increasing complexity also means that design, test and production costs reach levels where large volumes must be produced for a chip to be feasible. The time it takes to get a new product to the market (time-to market) thereby also increases. As envisioned in [1], this trend seems to make ASICs infeasible for the main bulk of applications the development time will simply be too long

For many applications a more general System-on-Chip (SoC) platform chip could be a viable solution. Such a SoC platform would contain many different IP-cores including RAMs, CPUs, DSPs, IOs, FPGAs and other coarse and fine grained programmable IP-cores.

The communication is provided by means of a flexible communication infrastructure in the form of a Network-on-Chip (NoC) [2, 3]. This allows the same SoC platform to be used in a wide range of different applications and thereby increases the production volume.

As the same SoC platform is to be used for many different applications, the NoC must be able to support a wide range of bandwidth and Quality-of-Service (QoS) requirements. The requirements of the applications can be very different, and the NoC must therefore be very flexible. Currently, the only way to provide such flexibility is to employ a large packet-switched NoC with an over-engineered total bandwidth capacity. Such a NoC would take a significant part of the SoCs silicon area and only a fraction of its capacity is utilized by a given application

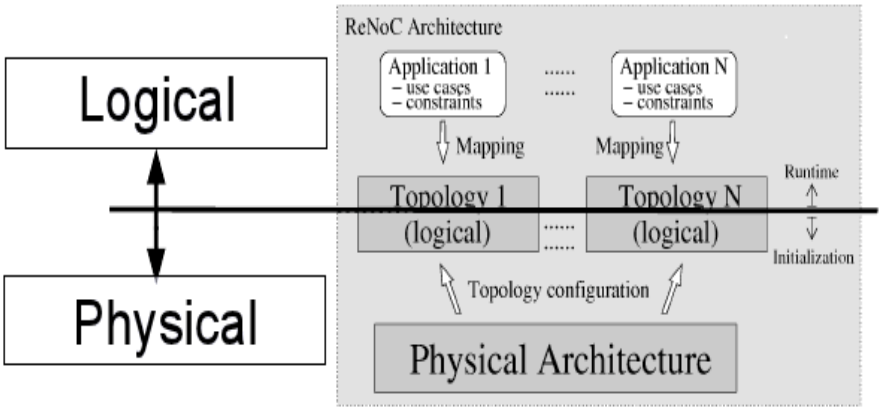


Figure 1. The ReNoC architecture enables a logical network topology to be configured by the application running on the physical SoC platform.

The topology switches are implemented using physical circuit-switching as found in FPGAs, to minimize the power consumption and area overhead. The motivation for inserting a configurable layer below existing NoC architectures is that physical circuit switching is far more efficient (in terms of area, power and speed) than intelligent, complex packet-switching which therefore must be avoided when possible. The communication requirement for the application is therefore used to configure a logical topology that minimizes the amount of packet-switching.

II. TERMINOLOGY

This section introduces basic terms used in the paper. Physical architecture is the actual physical layout of the NoC architecture as shown in the figure 1.Logical topology is the topology that is configured on top of the physical architecture as shown in figure 1. This is the topology as it is viewed by the application. Physical circuit-switching is used to denote a dedicated physical connection. Once the connection is set up, data can be transferred through the connection without any header information and no routing or arbitration is needed. This is not to be confused with virtual circuit-switching such as Time-Division Multiplexing (TDM).Router is used to denote any packet-switched router. The route might implement Quality-of-Service features such as TDM and/or prioritization of data.

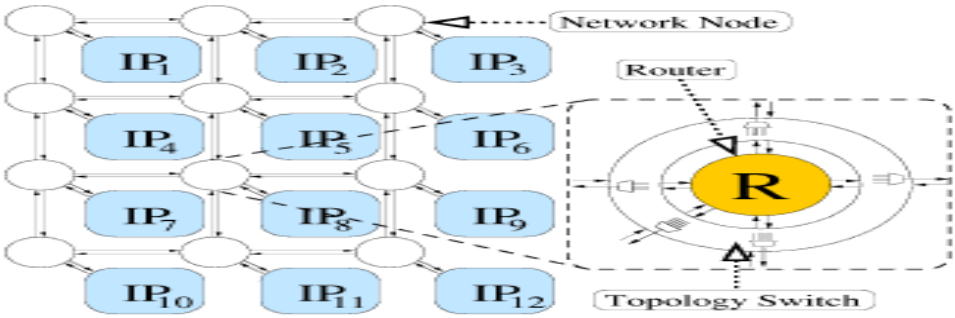


Figure 2. A simple physical architecture where network nodes are connected in a 2D mesh topology. A network node consists of a router that is wrapped by a topology switch.

The fundamental ideas of ReNoC are best explained through an example. For this, figure 2 shows a physical architecture consisting of network nodes connected by links in an 2D mesh topology. Each network node consists of a conventional NoC router which is wrapped by a topology switch. The topology switches are used to connect links and routers into a logical topology and they thereby allow different application-specific logical topologies to be configured on top of the same physical architecture. Figure 3 shows two examples of logical topologies that can be created by configuring the topology switches appropriately. As seen, it is possible to form long logical links connecting: (i) Any two IP-blocks, (ii) any two routers, and (iii) any IP-core and router. The physical distance between the IP-core/router does not matter, as long as a logical link can be established. Figure 3 illustrates that it is possible to configure logical topologies that are very different from the basic 2D mesh. If desired, it is also possible to configure a logical topology which is a 2D mesh.

III HETEROGENEOUS PHYSICAL ARCHITECTURE

In this architecture we are using routers and topology Switches separately as well as combined also taking for network nodes and so the architecture is complex

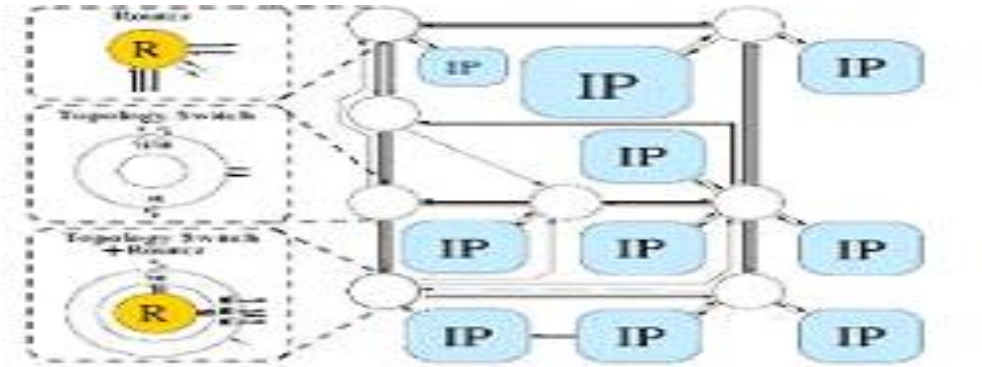


Figure 3 : Example of a complex, heterogeneous, physical architecture

Network nodes can contain a router, a topology switch, or both. Several IP-cores can be connected to the same network node, several link scan exist between network nodes, and IP-blocks can be directly connected.

The architecture is not restricted to a specific router. The only requirement is that the link width, including wires for flow-control, matches the ports on the router. In principle the communication protocol is defined by the routers and the topology switches and links act as passive circuit-switched interconnects. This means that the architecture can be used in combination with any existing router. The routers can contain Virtual Channels (VC), Quality of-Service (QoS) implementations such as TDM, queuing buffers, and can be implemented using synchronous or asynchronous circuit techniques. The ReNoC concept can thus be used with existing routers including Mango [8], and Xpipes [9].

IV VOPD APPLICATION AS BENCHMARK

Input can be used as HDTV or raw data input streams or real-time video streams as an example for application of VOPD which is used as bench mark circuit .Tools using for this process is Quartus II, Sopc builder, niosII

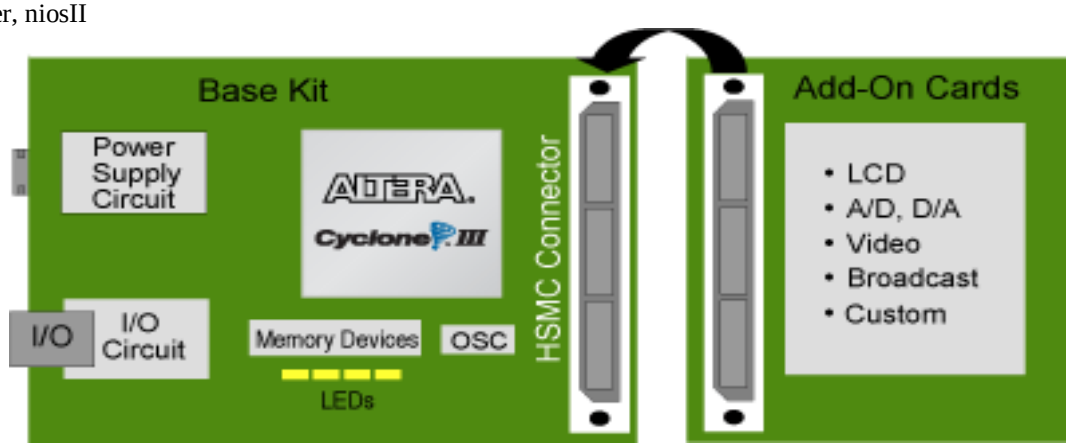
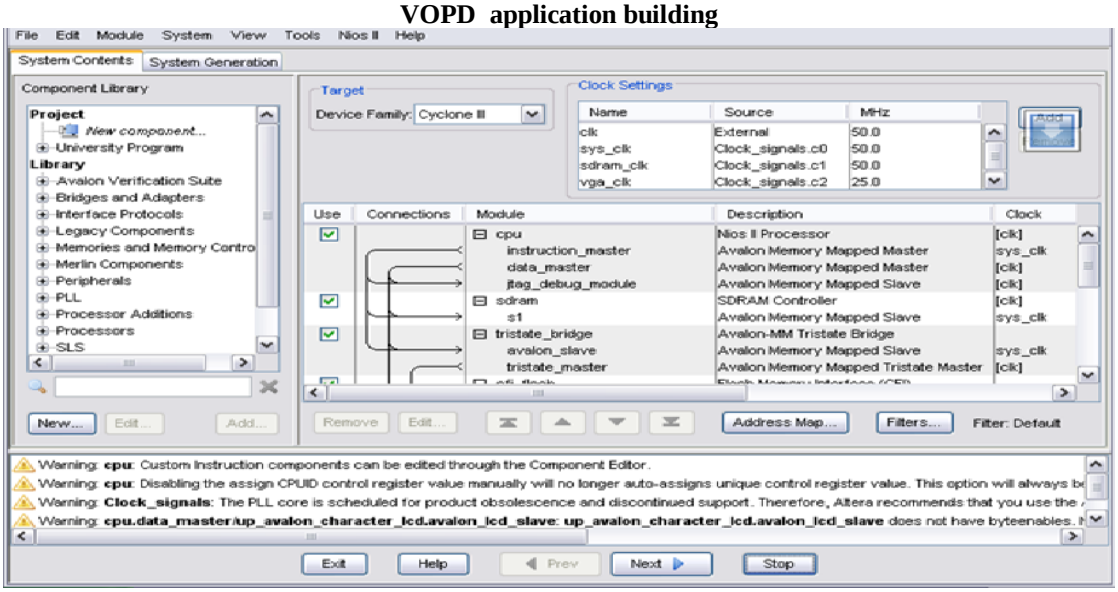


Figure 4: overview of cyclone III embedded development kit

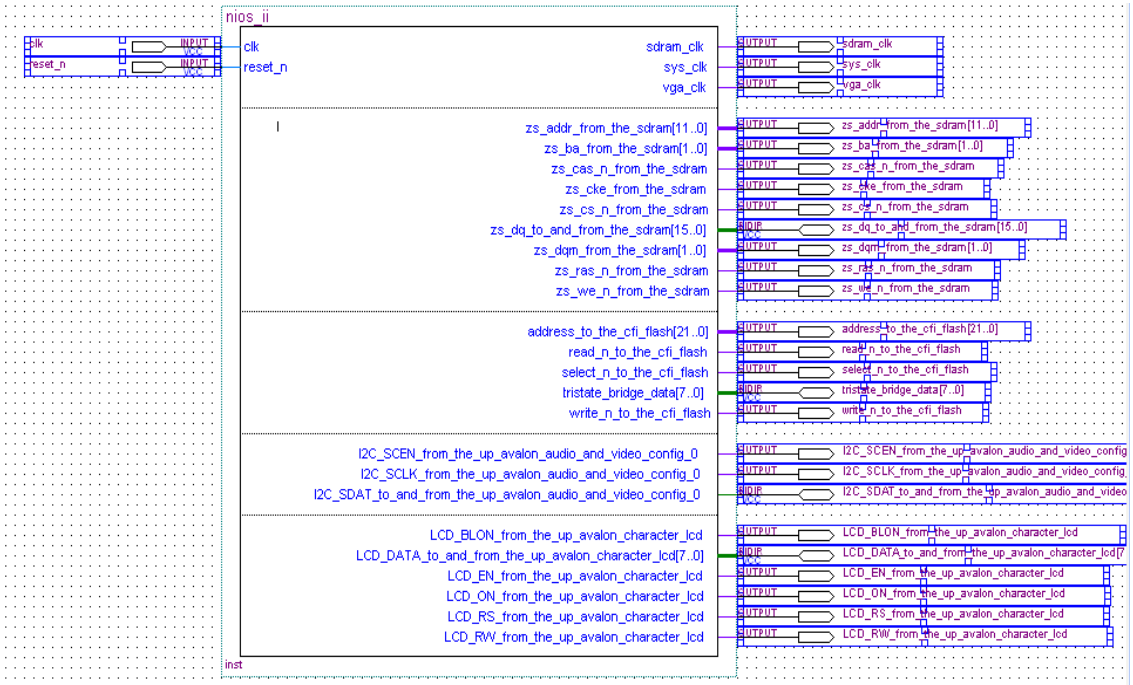
This is an advanced cyclone III embedded development kit for video processing which have a extra daughter card interfaced with HSME connector and daughter card includes RS232 serial port and video input port and video output serial ports so that implementation of video processing is possible, apart from that this base kit have a LCD display to view the output

Through Synopsys tools (.i.e, Design vision, prime time) we can estimate optimised area and power of our design but can't be implemented in fpgas before chip fabrication. so in order to check our designs before fabrication we are going to quartus II and nios II softwares for estimations of optimised area and power , as well as we can implement on fpgas

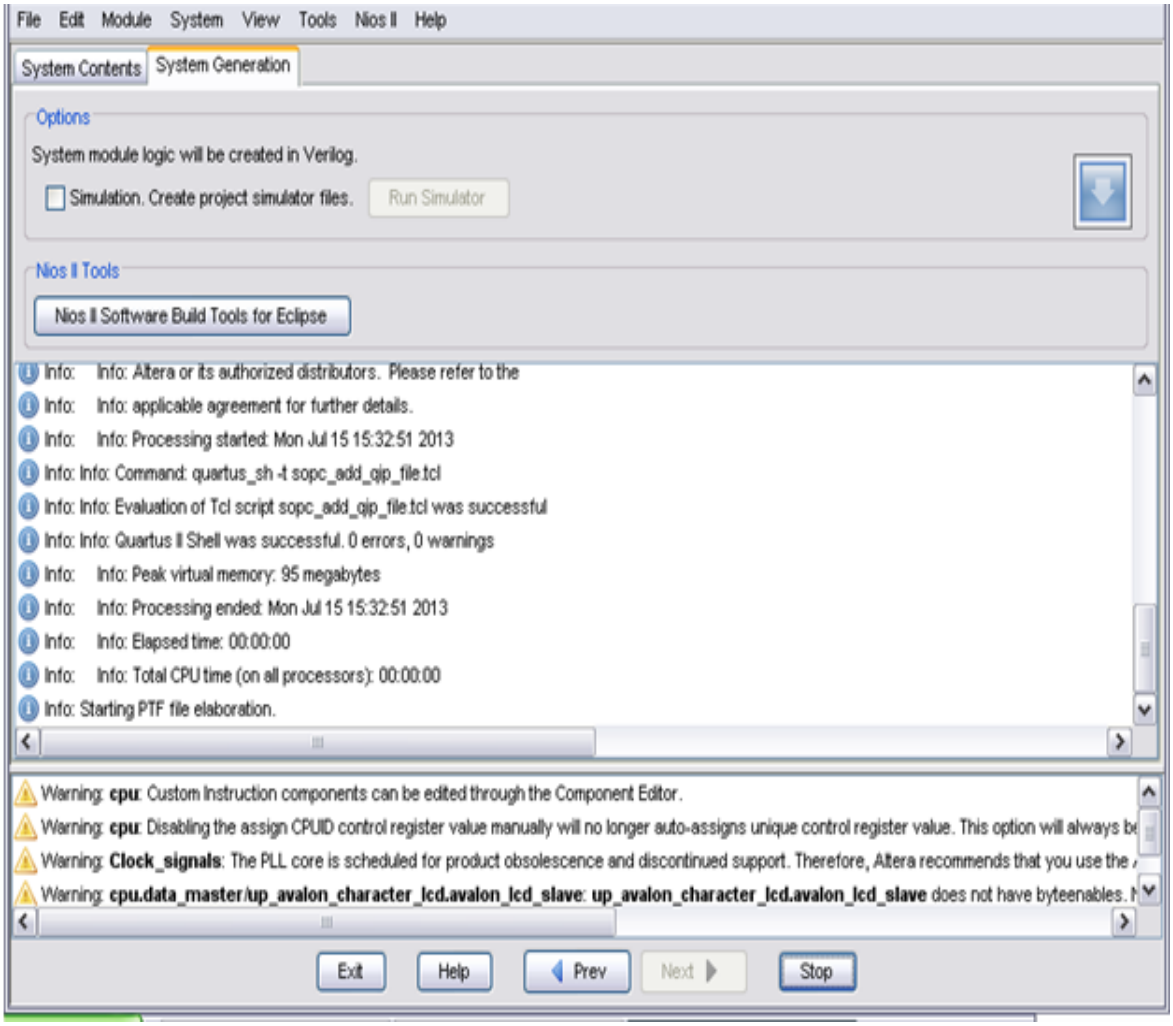
VOPD application building



VOPD Schematic



Result for SoC Generation



Results for SoC Implementation

Flow Summary

Flow Status	Successful - Sun Jul 14 05:27:19 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DE2_Zip_File_System2
Top-level Entity Name	nios_ii
Family	Cyclone III
Device	EP3C120F780C7
Timing Models	Final
Met timing requirements	N/A
Total logic elements	4,467 / 119,088 (4 %)
Total combinational functions	3,914 / 119,088 (3 %)
Dedicated logic registers	2,798 / 119,088 (2 %)
Total registers	2915
Total pins	91 / 532 (17 %)
Total virtual pins	0
Total memory bits	64,896 / 3,981,312 (2 %)
Embedded Multiplier 9-bit elements	4 / 576 (< 1 %)
Total PLLs	1 / 4 (25 %)

Power estimated for device

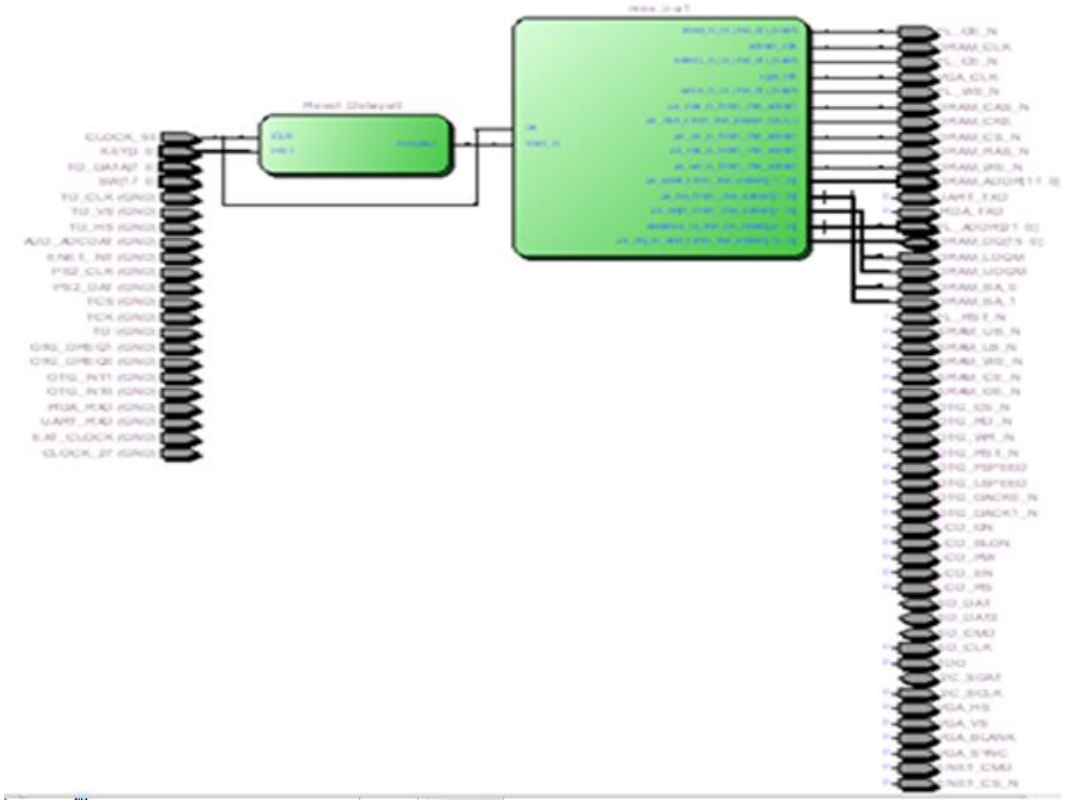
PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Sun Jul 14 05:36:49 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DE2_Zip_File_System2
Top-level Entity Name	nios_ii
Family	Cyclone III
Device	EP3C120F780C7
Power Models	Final
Total Thermal Power Dissipation	163.11 mW
Core Dynamic Thermal Power Dissipation	1.05 mW
Core Static Thermal Power Dissipation	105.14 mW
I/O Thermal Power Dissipation	56.92 mW

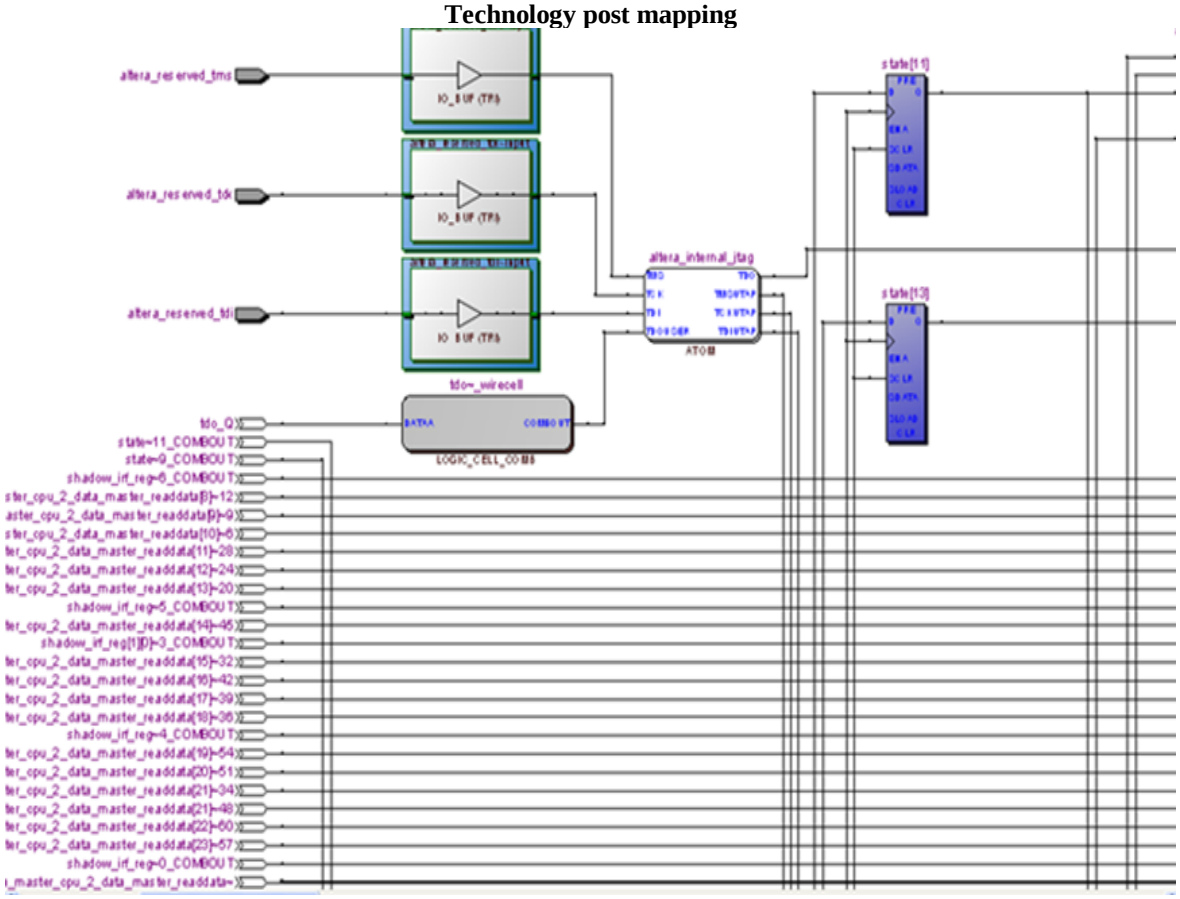
Verilog coding

```
250   input           TD_VS;                  //  TV Decoder V_SYNC
251   output          TD_RESET;               //  TV Decoder Reset
252   input           TD_CLK;                 //  TV Decoder Clock
253   ////////////////////    GPIO    ////////////////////////////
254   inout   [35:0]  GPIO_0;                 //  GPIO Connection 0
255   inout   [35:0]  GPIO_1;                 //  GPIO Connection 1
256   wire CPU_RESET;
257
258 Reset_Delay u0 (
259     .iRST(KEY[0]),
260     .iCLK(CLOCK_50),
261     .oRESET(CPU_RESET)
262   );
263
264
265 nios_ii u1 (
266     .clk                                (CLOCK_50),
267     .sdram_clk                          (DRAM_CLK),
268     .sys_clk                            (),
269     .vga_clk                            (VGA_CLK),
270     .reset_n                            (CPU_RESET),
271     .select_n_to_the_cfi_flash          (FL_CE_N),
272     .address_to_the_cfi_flash           (FL_ADDR),
273     .read_n_to_the_cfi_flash            (FL_OE_N),
```

RTL schematic



Technology post mapping

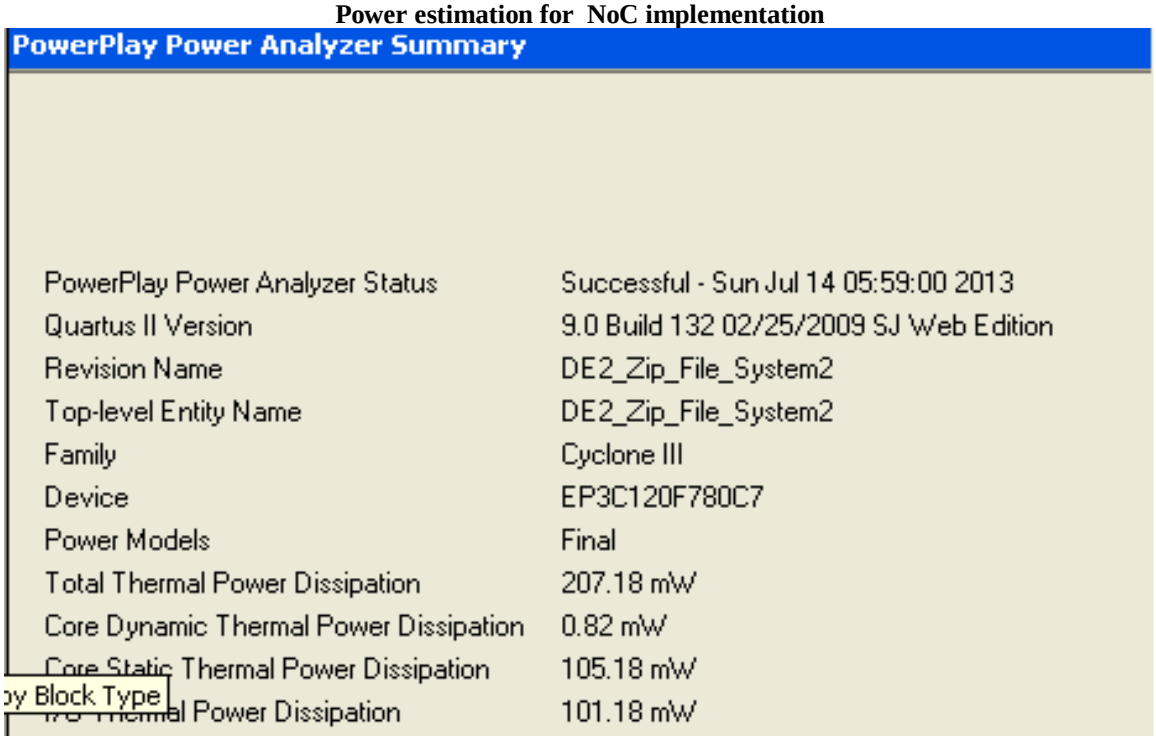


NoC results for area

Flow Summary

Flow Status	Successful - Sun Jul 14 05:54:52 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DE2_Zip_File_System2
Top-level Entity Name	DE2_Zip_File_System2
Family	Cyclone III
Device	EP3C120F780C7
Timing Models	Final
Met timing requirements	N/A
Total logic elements	4,506 / 119,088 (4 %)
Total combinational functions	3,956 / 119,088 (3 %)
Dedicated logic registers	2,831 / 119,088 (2 %)
Total registers	2924
Total pins	426 / 532 (80 %)
Total virtual pins	0
Total memory bits	64,896 / 3,981,312 (2 %)
Embedded Multiplier 9-bit elements	4 / 576 (< 1 %)
Total PLLs	1 / 4 (25 %)

Power estimation for NoC implementation



V. NETWORK TOPOLOGIES

The following architectures are used for comparison:

Static mesh:

A static 2D mesh topology used as reference. It is similar to the topology shown in figure 2 where each network node contains a statically connected router.

ReNoC mesh:

The ReNoC architecture that is configured to provide a 2D mesh logical topology similar to Static Mesh This configuration is used to characterize the Overhead of the topology switches.

ReNoC specific**:**

The ReNoC architecture that is configured with the application specific topology

VI. CONCLUSION AND FEATURE WORK

We are using vopd application as bench mark circuit here so we can use digital video DVD player as input and also we can give raw data as input which is real time input directed source from CMOS sensor video This work can be extended through wireless approach to get process of network on chip for video object plane decoder application

This can be extended to further research to get blue ray DVD used in DVD player changes to IC chip, utilized for home theater application and also we can use for implementing applications like multimedia pcs ,video conferencing

REFERENCE

[1]. P. Magarshack and P. G. Paulin, "System-on-chip beyond the nanometer wall," in DAC 03: Proceeding of the 40th conference on Design automation. NewYork, NY, USA: ACM Press2003,

[2]. W. J. Dally and B. Towles, "Route packets, not wires: On-chip interconnection networks," in Design Automation, 2001

[3]. G. de Micheli and L. Benini, "Networks on chip: A new paradigm for systems on chip design," 2002

[4]. W. J. Dally, "'enabling technology for on-chip interconnection networks' keynote presentation at 'the 1st acm/ieee international symposium on networks-on-chip2007

[5]. A. Banerjee, R. Mullins, and S. Moore, "A power and energy exploration of network-on-chip architectures," 1st international symposium, 2007.

[6]. M. Modarressi, "A reconfigurable topology for NoCs," Tech. Rep. TR-HPCAN10-2, 2010.

[7]. D. Bertozzi, A. Jalabert, S. Murali, R. Tamahankar,S.Stergiou, L. Benini, and G. De Micheli, "NoC synthesis flow for customized domain specific multiprocessor systems-on-chip," IEEE Trans. Parallel Distrib. Syst., vol. 16, no. 2, pp. 113–129, Feb. 2005.

[8]. T. Bjerregaard and J. Sparsø, "A router architecture for connection-oriented service guarantees in the mango clockless network on-chip," in Proc. Design Automation and Test in Europe (DATE'05), ACM sigda, 2005, pp. 1226–1231.

[9]. D. Bertozzi and L. Benini, "Xpipes: a network-on-chip architecture for gigascale systems-on-chip," Circuits and Systems Magazine, IEEE, vol. 4, no. 2,pp.1101–1107,2004.